IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT

In re application of: Jeffrey Craig et al.

Attorney Docket No.: SANDP007

Application No.: Unknown

Examiner: Unknown

Filed: Unknown

Group: Unknown

Title: METHOD AND APPARATUS FOR DYNAMIC DEGRADATION DETECTION

CERTIFICATE OF EXPRESS MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service"Express Mail Post Office to Addressee" service under 37 CFR § 1.10 on the date indicated below and is addressed to: BOX PATENT APPLICATION Assistant Commissioner for Patents, Washington, DC 20231 on January 16, 2002.

Signed: ______________________
Jack Limper

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to substantive examination of the above-referenced patent application, please enter the following amendments and remarks

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 9, at line 28, with the following paragraph.

Referring next to Fig. 1b, non-volatile memory device 120 will be described in more detail in accordance with an embodiment of the present invention. As described above, non-volatile memory device 120 includes non-volatile memory 124 and memory control system 128. Memory 124 and control system 128, or controller, are primary components of non-volatile memory device 120. Memory 124 may be an array of memory cells formed on a semiconductor substrate, wherein one or more bits of data are stored in the individual memory cells by storing one of two or more levels of

charge on individual storage elements of the memory cells. A non-volatile flash electrically erasable programmable read only memory (EEPROM) is an example of a common type of memory for such systems. One suitable flash EEPROM system is described in U.S. Patent No. 5,602,987, which is incorporated herein by reference in its entirety.

Please replace the paragraph beginning on page 10, at line 29, with the following paragraph.

Array 11 is divided into a large number of BLOCKS 0 – N of memory cells. As is common for flash EEPROM systems, the block may be the unit of erase. That is, each block may contain the minimum number of memory cells that are erased together. It should be appreciated that a unit of erase may be commonly referred to as a sector, a block, a page, or any similar term as known to those skilled in the magnetic and semiconductor data storage arts, or similar terms known to those skilled in other data storage arts. Each block is typically divided into a number of pages, as also illustrated in Fig. 1b. A page may be the unit of programming. That is, a basic programming operation generally writes data into a minimum of one page of cells. One or more sectors of data are typically stored within each page. As shown in Fig. 1b, one sector includes user data and overhead data (OH). Overhead data typically includes an error correction code (ECC) that has been calculated from the user data of the sector. A portion 23 of the control system 13 calculates the ECC when data is being programmed into array 11, and also checks the ECC when data is being read from array 11. Alternatively, the ECCs are stored in different pages, or different blocks, than the user data to which they pertain.

Please replace the paragraph beginning on page 13, at line 28, with the following paragraph.

A spare sector counter may generally be maintained by a memory controller, *e.g.*, memory control system 128 of Fig. 1. In one embodiment, when a memory device such as a flash memory card is manufactured, a number of sectors or blocks in the memory device are set aside as spare sectors, a threshold is determined, and the spare sector counter is initiated. That is, at manufacturing time, in addition to allocating spare sectors, a reserved system sector may be written with a counter which effectively defines the number of spare sectors which remain on the memory device, and a

minimum number of spare sectors which are to remain as spare sectors to prevent an end-of-life indication is defined. The threshold that is determined may also be written into a reserved system sector at manufacturing time. Both the counter and the threshold may be stored as bits within the reserved system sector.

REMARKS

The Specification has been amended for clarity.

In view of the above, the Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this preliminary amendment, the Commissioner is authorized to charge such fees to Deposit Account 50-1652 (Order No. SANDP007).

Respectfully submitted,
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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph beginning on page 9, at line 28, was replaced with the following paragraph.

Referring next to Fig. 1b, non-volatile memory device 120 will be described in more detail in accordance with an embodiment of the present invention. As described above, non-volatile memory device 120 includes non-volatile memory 124 and memory control system 128. Memory 124 and control system 128, or controller, are primary components of non-volatile memory device 120. Memory 124 may be an array of memory cells formed on a semiconductor substrate, wherein one or more bits of data are stored in the individual memory cells by storing one of two or more levels of charge on individual storage elements of the memory cells. A non-volatile flash electrically erasable programmable read only memory (EEPROM) is an example of a common type of memory for such systems. One suitable flash EEPROM system is described in U.S. Patent No. 5,602,987, which is incorporated herein by reference in its entirety.

The paragraph beginning on page 10, at line 29, was replaced with the following paragraph.

Array 11 is divided into a large number of BLOCKS 0 – N of memory cells. As is common for flash EEPROM systems, the block may be the unit of erase. That is, each block may contain [contains] the minimum number of memory cells that are erased together. It should be appreciated that a unit of erase may be commonly referred to as a sector, a block, a page, or any similar term as known to those skilled in the magnetic and semiconductor data storage arts, or similar terms known to those skilled in other data storage arts. Each block is typically divided into a number of pages, as also illustrated in Fig. 1b. A page may be [is] the unit of programming. That is, a basic programming operation generally writes data into a minimum of one page of cells. One or more sectors of data are typically stored within each page. As shown in Fig. 1b, one sector includes user data and overhead data (OH). Overhead data typically includes an error correction code (ECC) that has been calculated from the user data of the sector. A portion 23 of the control system 13 calculates the ECC when data is being programmed into array 11, and also checks the ECC when

data is being read from array 11. Alternatively, the ECCs are stored in different pages, or different blocks, than the user data to which they pertain.

The paragraph beginning on page 13, at line 28, was replaced with the following paragraph.

A spare sector counter may generally be maintained by a memory controller, *e.g.*, memory control system 128 of Fig. 1. In one embodiment, when a memory device such as a flash memory card is manufactured, a number of sectors or blocks in the memory device are set aside as spare sectors, a threshold is determined, and the spare sector counter is initiated. That is, at manufacturing time, in addition to allocating spare sectors, a reserved system sector may be written with a counter which effectively defines the number of spare sectors which remain on the memory device, and a minimum number of spare sectors which are to remain as spare sectors to prevent an end-of-life indication is defined. <u>The threshold that is determined may also be written into a reserved system sector at manufacturing time. Both the counter and the threshold may be stored as bits within the reserved system sector.</u>